X-band Digital Receiver for the New Horizons Spacecraft[1,2]

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Abstract—A low-power X-band digital uplink receiver has been developed by the APL for NASA's planned New Horizons mission to Pluto and the Kuiper Belt, which is scheduled to launch in January 2006 with a Pluto encounter as early as 2015. The Uplink Receiver provides X-band carrier tracking, command detection/demodulation, critical command decoding, ranging tone demodulation, and built-in radiometrics modes. The primary RF carrier tracking, command detection, and ranging requirements are similar to those of predecessor deep space RF systems, including both the small deep space transponder (SDST) and CONTOUR RF transceiver systems. Additional design requirements for radioscience compatibility and reduced power consumption led to a new design approach. The new receiver design makes use of digital processing techniques and revised system architecture to meet these new requirements, while at the same time enhancing performance and flexibility over predecessor systems. A 53% to 68% reduction in secondary power consumption over comparable predecessor systems has been achieved. This paper provides a detailed description of the new low-power digital receiver design.

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1. INTRODUCTION

The Uplink Receiver has been designed into the New Horizons RF transceiver system [1] housed in an Integrated Electronics Module (IEM), with heritage from both the TIMED and CONTOUR missions. The receiver form factor is a heritage 15 x 23 cm plug-in card in the IEM.

The new coherent receiver design is based on experience gained in noncoherent transceiver systems from the TIMED and CONTOUR missions [2], while at the same time making use of enabling technologies in use by the commercial electronics industry. The resulting design is therefore a balance of modern commercial electronics with the high reliability required for deep space communications systems.

The X-band uplink signal (**Figure 1**) to be received is generated by an earth station in the Deep Space Network (DSN) and nominally consists of several components: 1) a phase-modulated residual carrier, 2) a 16 KHz sinusoidal subcarrier that is binary phase-shift-key (BPSK) modulated with uplink command data, and 3) sequential or pseudorandom noise (PN) modulated ranging tones. The residual carrier is used by Uplink Receiver to lock onto the composite signal and track out Doppler effects, while also providing navigation data critical to the noncoherent navigation system. The data modulated subcarrier is used by the command detection unit to lock onto and demodulate uplink command data while tracking out Doppler effects. The ranging tones are demodulated or regenerated and provided to the Downlink Card for use in the turnaround ranging system.

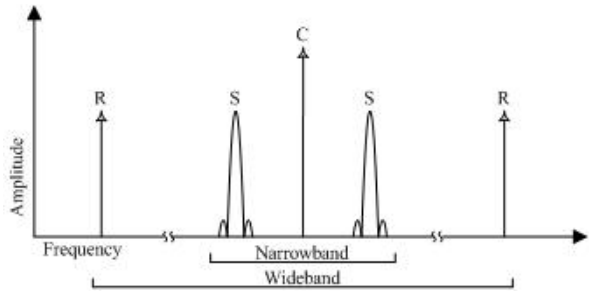

Figure 1 – Nominal Composite Uplink Signal Diagram
C = carrier, S = subcarrier/command data, R = ranging

[1] 0-7803-8155-6/04/$17.00© 2004 IEEE
[2] IEEEAC paper #1031, Version 4, Updated December 15, 2003

The Uplink Receiver IEM card (**Figure 2**) is an assembly consisting of three printed circuit boards (PCB) mounted to an aluminum heat sink. On one side, a multilayer, polyimide PCB contains the circuitry for the radio frequency (RF), intermediate frequency (IF), analog, and digital sections of the X-band carrier tracking receiver, ranging tone demodulation, and a wideband IF channel for radiometrics modes. Attached to this polyimide PCB is an RF downconverter board, which consists of a temperature stable microwave substrate and most of the receiver's X-band and RF circuitry. On the other side of the card assembly, a second multilayer, polyimide PCB contains the required circuitry for the command detector unit (CDU) and the critical command decoder (CCD).

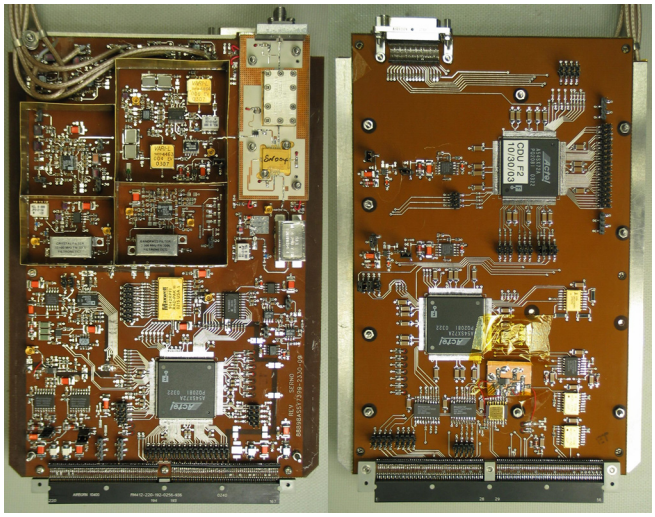

Figure 2 – Photographs of Prototype Uplink Receiver a) digital receiver side, b) baseband side (CDU and CCD)

The following sections discuss the basic design of the digital Uplink Receiver's various subsystems. A summary of the primary performance achievements of the new receiver design is also presented.

2. SYSTEM DESIGN

The core receiver design uses a classic double-conversion, superheterodyne approach, with the addition of requirements for carrier tracking and noncoherent automatic gain control (AGC). The entire Uplink Receiver system (**Figure 3**) is best described by separating functions into four distinct sections: the external RF circuitry, the RF board, the RF/analog subsystem, and the digital subsystem. The external RF circuitry, RF board, and RF/analog subsystem will be discussed in Section 3 and the digital subsystem will be discussed in Section 4. Each of these subsystems provides a critical role in the performance of the overall system, which is designed around a critical function of the Uplink Receiver, X-band carrier tracking and AGC. In order for the Uplink Receiver to function properly, the carrier tracking and AGC systems must first be operational, both of which make use of a narrowband downconversion chain and the digital subsystem.

Noncoherent Automatic Gain Control

The noncoherent AGC system is based on a digital power detector and loop filter that feeds a digital-to-analog converter (DAC). The output voltage generated by the DAC is used to vary the gain in the receiver's narrowband downconversion system. The noncoherent AGC system detects the total power (signal and noise) in the narrowband 2nd IF channel for automatic carrier tracking loop bandwidth adjustment. This bandwidth adjustment is achieved through a limiting effect, defined by α (Equation 1).

$$\alpha = [SNR/(SNR+4/\pi)]^{1/2} \qquad (1)$$

α is the signal suppression due to the noncoherent AGC system [3], and SNR is the signal-to-noise ratio in the narrowband 2nd IF channel. Since the wideband 2nd IF is not sampled by an analog-to-digital converter (ADC), and doing so would add considerably more power consumption to the system, its gain is also controlled by the narrowband AGC system with an offset added in to minimize clipping in the final amplification stages due to the wider noise bandwidth. This open loop method of gain control in the wideband channel requires that subsystems that make use of this channel have enough dynamic range to accommodate the varying channel power compared to the narrowband channel. This wideband channel power variation is small when compared to the variation in signal amplitudes (due to the noncoherent AGC system) that the various subsystems are required to operate on. One of the advantages of using a noncoherent AGC system is that power detection occurs in a much wider bandwidth than in coherent detection systems, allowing the AGC system to respond and settle before the carrier tracking loop "sees" the carrier during swept carrier acquisition operations. In addition, noncoherent AGC telemetry may be downlinked to provide useful information about the received uplink signal strength regardless of carrier lock status.

Carrier Acquisition and Tracking

The carrier tracking loop is a long loop, type I phase-locked loop (PLL) designed to track Doppler-induced changes in frequency of the X-band uplink carrier received at the spacecraft. The loop filter, which is based on an active imperfect integrator and resides in the digital subsystem, causes the carrier tracking loop to approximate type II PLL behavior [3]. The carrier tracking PLL uses the receiver's narrowband downconversion chain, ADC and digital demodulation circuits, digital channel select and loop filters, and a direct digital synthesizer (DDS)-based carrier tracking frequency reference. The digital subsystem demodulates the downconverted carrier to baseband to provide phase detection of the fixed 2.5 MHz IF, which is then fed through the digital channel select and loop filters. The performance

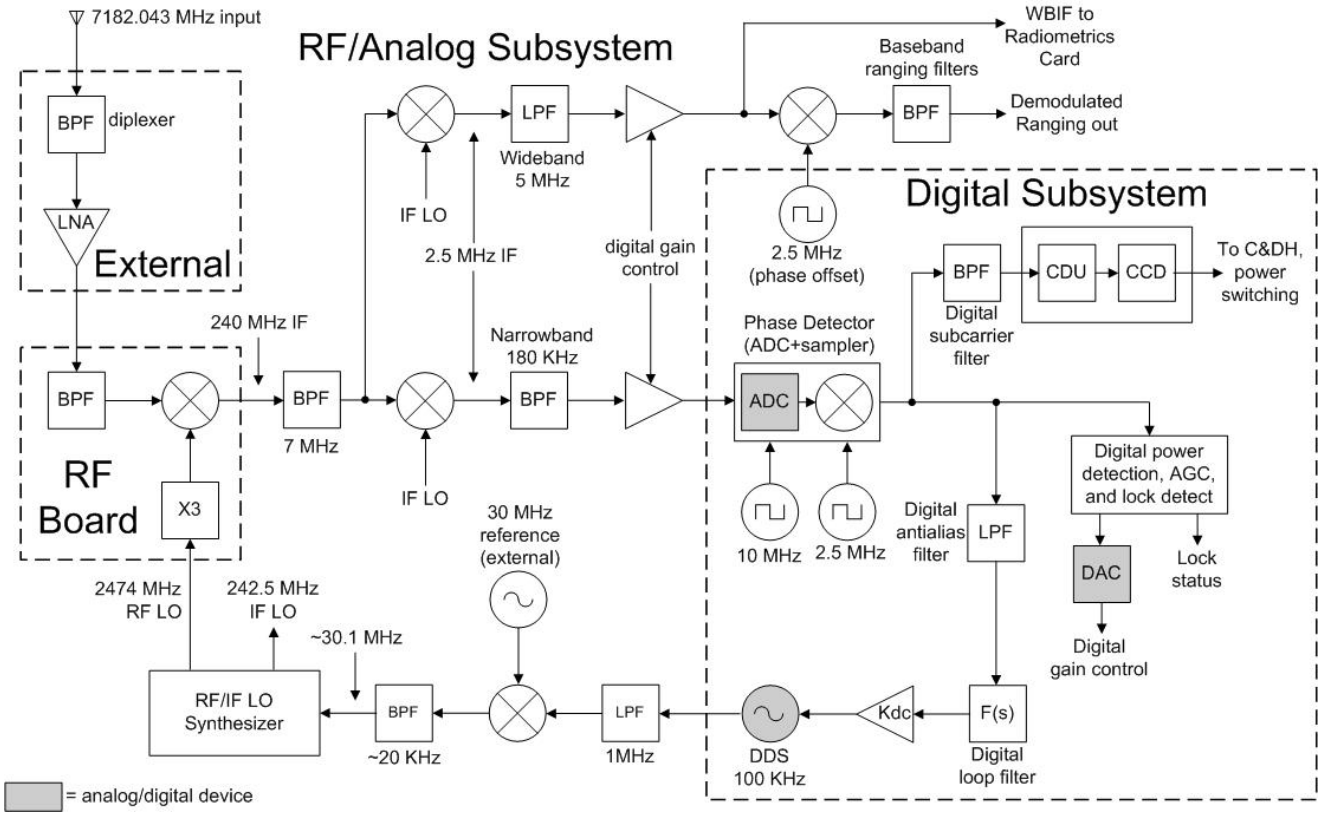

Figure 3 - Uplink Receiver System Block Diagram

of the closed-loop carrier tracking system is set by the gain and bandwidth of this loop filter in addition to DC gain throughout the feedback system. The DDS output frequency of approximately 100 KHz is mixed with the 30 MHz spacecraft frequency reference to obtain approximately 30.1 MHz. The resultant 30.1 MHz signal is used to drive a dual RF/IF frequency synthesizer integrated circuit (IC), which generates both a RF local oscillator (LO) and IF LO. These LOs are used in the receiver's downconversion system, both of which move in response to shifts in the DDS frequency to achieve carrier tracking; the result is a variable 1st IF of approximately 240 MHz and a fixed 2nd IF of exactly 2.5 MHz relative to the 30 MHz spacecraft reference. The 30 MHz spacecraft reference is an Ultrastable Oscillator (USO) [1], which is also designed in-house at the APL.

The primary design drivers for the carrier tracking system are: carrier acquisition threshold, tracking range, and sweep rate. In order to provide wide range, high rate, carrier tracking and acquisition while maintaining a carrier acquisition threshold of better than -155 dBm (referenced to the LNA input), the closed-loop carrier tracking bandwidth is automatically adjusted for decreasing input carrier power. The noncoherent AGC system provides this bandwidth adjustment through the suppression factor α (Equation 1) and its effective reduction of the open-loop gain, G(s), in the carrier tracking system.

$$G(s) = [\alpha \times K \times F(s)]/s \qquad (2)$$

where K is the DC gain throughout the carrier tracking PLL system and F(s) is the response of the digital loop filter. The resultant closed-loop response is:

$$H(s) = G(s) / [1 + G(s)] \qquad (3)$$

Since the suppression factor affects both the natural frequency (ω_n) and damping factor (ξ) across the entire range of SNR in the narrowband IF channel, careful design of the closed-loop PLL system must ensure stability for all conditions [3]. For low signal SNR in the narrowband IF bandwidth, α approaches zero. At the required threshold of -155 dBm ($\alpha \approx 0.015$), the loop is designed for a closed-loop, two-sided noise bandwidth ($2B_L$) of approximately 18 Hz and $\xi \approx 0.5$. At a high SNR, α approaches unity, which results in $2B_L \approx 565$ Hz and $\xi \approx 3.93$. The result is high carrier tracking rate capability over a wide frequency range for stronger input carrier power levels, with a reduction in tracking rate/range capability to achieve the required threshold performance as the input carrier power level decreases and $2B_L$ is narrowed

Command Detection and Decoding

Once the carrier tracking system has achieved lock during mission operations, the earth station (E/S) phase modulates

a data modulated subcarrier onto a residual X-band carrier. Once the composite X-band signal has been downconverted to the 2nd IF through the receiver, the digital subsystem demodulates the narrowband channel to baseband. The digital baseband data is filtered to select the 16 KHz subcarrier, which is then forwarded to the CDU for data demodulation and command detection. For the New Horizons mission, this subcarrier is binary phased shift key (BPSK) modulated with commands at data rates of 2000, 500, 125, and 7.8125 bps. The CDU locks to and tracks the subcarrier and demodulates the command data, passing data and clock over to the CCD. In the CCD, designated critical relay commands are decoded, detected, and immediately sent to the power switching system. The CCD also forwards all commands to the command and data handling (C&DH) system.

Radiometrics Modes

For the New Horizons mission, two critical radiometrics requirements were drivers in the Uplink Receiver system design: the Radioscience Experiment (REX) and the regenerative ranging subsystems [1]. Both of these radiometrics subsystems require use of the Uplink Receiver in order to function, and thus require special modes when operational.

A general purpose, 2.5 MHz, wideband IF (WBIF) channel is provided to both radiometrics subsystems, which demodulate and process this channel to achieve a variety of results. The WBIF is simply a wider bandwidth duplicate of the receiver's narrowband downconversion chain that is buffered and routed to the radiometrics subsystems. In addition, the Uplink Receiver's turnaround ranging demodulator (**Section 3**) makes use of this WBIF channel.

The regenerative (or PN) ranging subsystem is a new alternative to turnaround tone ranging and uses code correlators to regenerate a PN code that is part of the composite X-band signal transmitted by the uplink E/S. Turnaround tone ranging suffers from degradation in SNR due to the uplink E/S to spacecraft path loss, while regenerative ranging effectively eliminates this degradation [4]. The regenerative ranging subsystem's primary requirement of the Uplink Receiver is to provide a frequency and gain stable WBIF with approximately a 5 MHz noise bandwidth to pass the desired signal information.

The REX subsystem also makes use of the WBIF, but with the receiver's carrier tracking and AGC systems disabled. The LO frequencies and downconverter gains are fixed to predetermined values that may be reprogrammed during operations as necessary. The result is a fixed frequency downconversion system that can be used to measure phase/frequency differences between the received X-band carrier and the spacecraft's on-board USO during an occultation rendezvous with Pluto and Charon. In addition, a total power radiometer will measure the estimated noise temperature of Pluto. Since placing the receiver in this fixed frequency downconversion mode precludes uplink command detection, spacecraft autonomy and timeout timers are used to reset the receiver into its default carrier tracking mode when necessary.

Component Radiation Hardness

Since this Uplink Receiver design must exhibit radiation immunity consistent with the mission requirements (**Section 5**), particular attention was paid to the choice of each active component. Low power digital and mixed-signal ICs are a key enabling technology for this new design approach. Readily available commercial ICs of this nature tend to consist of high-density CMOS circuitry that is intrinsically susceptible to radiation-induced single event latchup (SEL) and upset (SEU) phenomenon. As a result, a two-pronged approach was taken to both develop radiation hardened components in-house and perform extensive radiation testing of readily available commercial components. Radiation testing included SEL, SEU, and total ionizing dose (TID). In addition, some already acceptable space qualified, radiation hardened components were identified and utilized.

3. RF AND ANALOG DESIGN

As previously mentioned, the core receiver design is based on a double conversion, superheterodyne architecture. The X-band signal received at the spacecraft's antenna is downconverterted through the receiver and processed to reconstruct uplink command data, turnaround ranging tones, the regenerative ranging PN code, or perform REX occultation and total power radiometer measurements. The receiver downconversion system is comprised primarily of RF and analog circuitry. Other RF and analog circuitry in the Uplink Receiver design includes generation of the carrier tracking frequency reference for the dowconverter's RF and IF LOs.

External RF Circuitry

The X-band uplink signal is received at one of the spacecraft's antennas and passed through a diplexer, which separates the uplink and downlink signals. The output of the diplexer is routed to a bandpass filter (BPF) that provides additional rejection of the X-band downlink signal to minimize interference with the Uplink Receiver. The X-band uplink signal is then routed to a low noise amplifier (LNA) that both sets the noise floor of the downconversion system and provides a significant portion of the gain required in the receiver. Placement of the LNA as close as possible to the spacecraft antenna switching network minimizes receiver noise figure. Power is supplied to the LNA by the Uplink Receiver through a bias tee and coaxial cable connected to the RF output of the LNA.

RF Downconverter Board

The RF downconverter board (**Figure 4**) provides several key functions, including the external LNA microstrip bias tee, band select/image reject filtering, the first downconversion stage, and amplification, tripling, and harmonic filtering of the RF LO. The RF LO is generated at approximately 2474 MHz by a fractional-N synthesizer located elsewhere on the Uplink Receiver and routed to the RF downconverter board. The RF LO is amplified, tripled in a multiplier IC, and harmonic filtered; the resultant 7.4 GHz signal is used as the LO for an active mixer, which completes the first downconversion stage of the receiver. The output of the first downconversion stage is the first IF signal, which is approximately 240 MHz.

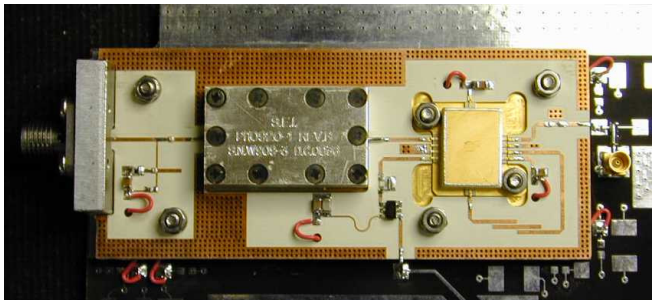

Figure 4 - Photograph of the RF Downconverter Board

The RF downconverter board contains a hybrid multi-chip module (MCM) (**Figure 5**) that contains the circuitry required for the tripler and active mixer in a hermetic RF package. The low-power tripler design is an in-house GaAs MESFET IC design [5], and the active mixer is a commercial GaAs pHEMT IC die that was qualified in-house for this mission.

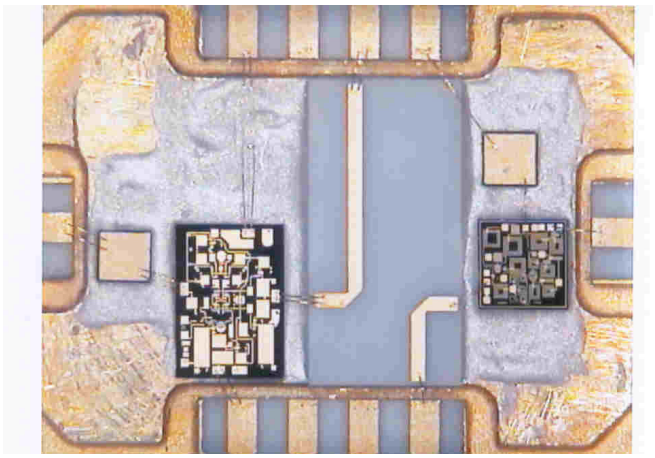

Figure 5 - Inside Photograph of the RF MCM

Carrier Tracking Frequency Reference

The carrier tracking frequency reference is used in the X-band carrier tracking system design that was discussed in Section 2. The output frequency and phase of a DDS is controlled by the digital subsystem to steer the LOs in the receiver downconversion system and achieve carrier tracking. The approximately 100 KHz DDS signal is mixed with the 30 MHz USO signal and filtered to remove the unwanted mixing products. The resultant approximately 30.1 MHz signal is used as a frequency reference for the RF and IF frequency synthesizer, which generates the RF and IF LOs. Any phase noise or modulation sidebands present on the 30.1 MHz tracking reference is increased due to multiplicative effects in the synthesizer and RF tripler circuits; the effective increase is approximately 20*log(N), where N is the effective multiplication factor from 30.1 MHz to the RF and IF LO frequencies. As a result of this multiplicative effect, particular requirements are placed on the filter design following the 100 KHz and 30 MHz mixing process; approximately 70 dBc rejection of the unwanted mixing products is required in this filter. A crystal filter is used to achieve the rejection required in the 30.1 MHz surface mount filter design.

Frequency Synthesizers

The RF and IF LOs are generated by a commercial, dual RF/IF frequency synthesizer IC. The RF section of the synthesizer is a fractional-N design and the IF section is an integer-N design. Both sections of the synthesizer use external commercial voltage controlled oscillators (VCO) and external discrete loop filters. The synthesizer loop filters were both designed to optimize phase noise and reduction of modulation sidebands in the receiver downconversion system. The frequency reference for this circuit is the 30.1 MHz carrier tracking frequency reference.

2nd Downconversion Circuitry

The 240 MHz 1st IF signal is bandpass filtered and split into two channels, one narrowband and one wideband. The narrowband channel is used for carrier tracking, automatic gain control, and command demodulation, while the wideband channel is used for turnaround ranging demodulation and generation of the WBIF channel to be used by the REX and regenerative ranging subsystems. Each channel contains a single-chip receiver IC, which provides the second downconversion stage, AGC amplification, and quadrature demodulation (used in wideband channel only).

Downconversion to the second IF of exactly 2.5 MHz makes use of the IF LO, which is generated at approximately 242.5 MHz by the IF synthesizer. Upon downconversion to the second IF, separate filtering of the wideband and narrowband channels is achieved via discrete

filter circuits external to the aforementioned receiver ICs. The 2.5 MHz narrowband IF (NBIF) channel is routed to the digital subsystem for sampling and further processing.

Ranging Demodulator

The 2.5 MHz WBIF channel is buffered and routed to the radiometrics subsystem for further processing. The 2.5 MHz WBIF is also demodulated via the aforementioned quadrature demodulator built into the single-chip receiver IC. The resultant baseband channel (or ranging channel) is filtered through several filters designed to limit the noise power in this channel as well as reduce the level of various demodulation products, while at the same time allowing the desired ranging tones to pass through with minimal phase and amplitude distortion. Since group delay variation in this channel degrades the overall ranging system performance, maximally flat delay filter designs such as Bessel filters were implemented where necessary. The output of this ranging channel is buffered and routed to the Downlink Card for modulation onto the downlink X-band carrier. In addition, the ranging channel has the capability to select and route either the demodulated ranging tones or the regenerated PN ranging code produced by the regenerative ranging subsystem to the Downlink Card within the RF transceiver system.

4. DIGITAL DESIGN

There are three sections to the digital processing subsystem of the receiver; the digital phase-locked-loop (DPLL), the CDU, and the CCD (**Figure 3**). Each section has a core RT54SX72A Field Programmable Gate Array (FPGA) device with supporting active and passive components. The DPLL section contains one FPGA, the narrowband ADC, a DAC for automatic gain control, and a DDS for carrier tracking. These four main components complete the digital portion of the carrier tracking, AGC, and lock detection circuits. The DPLL FPGA also performs the important task of demodulating and filtering the subcarrier from the downconverted and sampled carrier. The subcarrier channel is routed to the CDU, which is the second section of the digital processing system. The CDU circuitry is completely contained in one FPGA that performs subcarrier and symbol tracking. Once symbols are demodulated from the subcarrier, they are sent over to the CCD, which is the third section of the digital system. The CCD circuit consists of one FPGA and several digital buffering devices. This circuit decodes commands, executes critical switching commands, and passes commands and data to the main spacecraft processor. The CCD section will not be discussed here because it is considered part of the main processor system and only resides on the uplink card.

Digital Design Strategy

Within the DPLL and CDU sections there are three types of computational work being performed. The first function of each FPGA is managing the communications between several supporting digital devices, namely the ADC, DAC, DDS, CDU, CCD, carrier tracking PLL, and the frequency synthesizer. The second function of each FPGA is to report telemetry at a low rate for in flight telemetry, and at high rates for bench-top debugging purposes. Both of these tasks require fairly standard application of digital design and do not require functions more complicated than synchronizing two clocks of different rates or serializing parallel data. The third function of each FPGA is the computation of the integrators and filters for each digital data path.

The structure of all of the data paths was modeled after previous analog designs used in the CONTOUR Uplink Receiver [2]. The filter and integrator bandwidths were also directly modeled after the CONTOUR analog receiver design. The primary challenges in designing the digital subsystem were to minimize power consumption while realizing all of the required circuits in a limited number of FPGA gates. This design optimization was accomplished in several ways, the most important of which are frequency selection, algorithm efficiency, and the minimization of bit width in data paths.

Each data path update rate was chosen to be the lowest rate that did not interfere with that path's performance. A good rule of thumb is that the update rate of a data path should be $\geq$100 times the maximum desired frequency. These rates were also chosen to minimize frequency interference with the 2.5 MHz IF input. For instance, most of the I/O circuitry runs at 3.333333 MHz, which minimizes data harmonics produced and amplified in the analog second IF channel.

FPGA device space and power were both very limited; therefore the algorithm used to perform each block in **Figure 6** and **Figure 7** was optimized to balance both power consumption and gate usage for this application. Only five main adders in each FPGA execute all of the functional blocks. These adders are over clocked beyond the data path throughput rate and pipelined to perform multiple tasks. The most difficult algorithms to perform are the lowpass filters and the subcarrier bandpass filter. Each filter in the digital design is a bilinear transform of the original analog design that they are modeled after. The bandpass filter uses a direct form 1 configuration, and all of the lowpass filters use a direct form 2 transposed configuration [6]. To simplify each filter computation, no true multiplication is used, instead each filter coefficient is computed using a set of shifts and additions; this method greatly reduces FPGA resources, only slightly raises total power consumption, and yields multiplication results with more than acceptable accuracy.

Digital Phase-Locked Loop

A functional block diagram of the DPLL is shown in **Figure 6**. The only data input to the DPLL is the ADC that

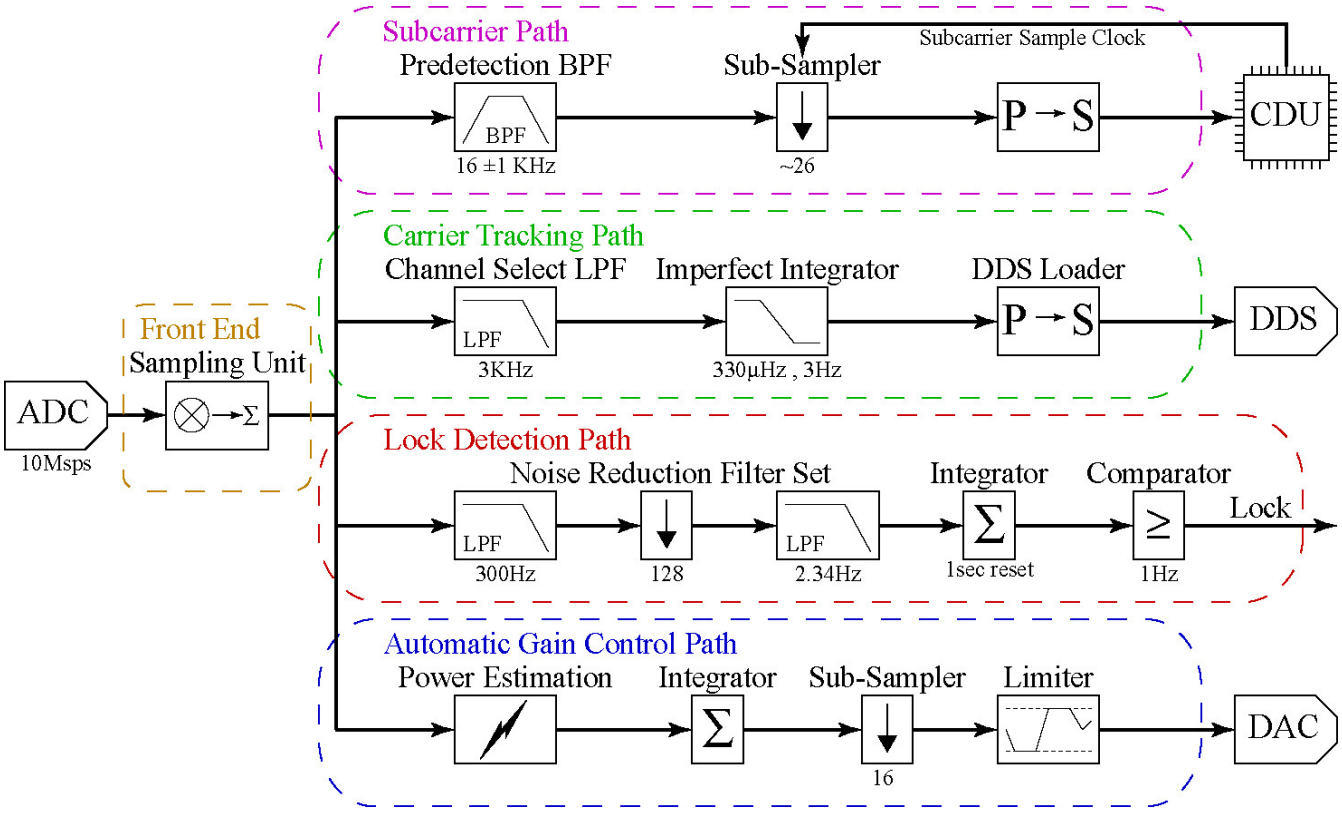

Figure 6 – DPLL Block Diagram

samples the narrow band second IF channel. Samples are taken on every peak and zero of the time domain carrier waveform (10 Msps). These samples are mixed with a 2.5 MHz square wave and separated into Zero and Peak paths (I and Q channels). The Sampling Unit outputs 3 busses; a sub-sampled set of the I channel, and 9 sample integrated values of the I and Q channels. These integrated values are the sum of 9 I samples and the sum of 9 Q samples. This integration is used to down sample the input data without losing any carrier information.

The Subcarrier Path uses the subsampled I channel to transfer information to the CDU at four times the subcarrier rate (64 KHz nominally); this path is band-pass filtered at a high rate with high precision to allow for very fine and accurate tracking of the subcarrier by the CDU. It should be noted that the 3 dB bandwidth of the subcarrier channel filter (±1 KHz) degrades the bit error performance of the 2000 and 500 bps uplink symbol rates. However, this filter is optimized for the lower command data rates and kept narrow to minimize interference caused by any spurs that may be close to the carrier or subcarrier frequency.

The Carrier Tracking Path uses the integrated I channel to detect the instantaneous phase error of the carrier and adjust the DDS frequency appropriately. The Imperfect Integrator is the loop filter for the carrier tracking PLL, which possesses a very large data path size to accommodate the slow time constants of this filter and maximum possible Doppler frequency offsets. The carrier *and* the subcarrier are present at the input to the Carrier Tracking Path. Therefore the Channel Select LPF is used to remove the subcarrier and select only the carrier signal of interest.

The Automatic Gain Control Path uses a combination of the I and Q channel to find the total power in the NBIF channel. The power estimation would ideally be computed by Equation 4, but has been simplified for space and power conservation to Equation 5 [7].

$$P_{channel} = (I^2 + Q^2)^{1/2} \quad (4)$$

$$P_{channel} = MAX(|I|, |Q|) + MIN(|I|, |Q|)/2 \quad (5)$$

This calculated instantaneous power value is compared to a fixed desired power value that is set based on the desired input levels to the ADC. The difference of these numbers is integrated continually, and the integrated power difference is sub-sampled and used as the gain control voltage.

The Lock Detection Path uses the Q-channel to detect the coherent amplitude of the carrier. The instantaneous amplitude is heavily low-pass filtered, and then compared to a fixed threshold to provide a single-bit lock indication. The indication is updated once per second.

Command Detector Unit

A complete functional CDU block diagram is shown in **Figure 7**. The Sampling Unit works exactly the same as the DPLL counterpart. Every zero and peak of the subcarrier is sampled, mixed down to baseband, separated into I and Q

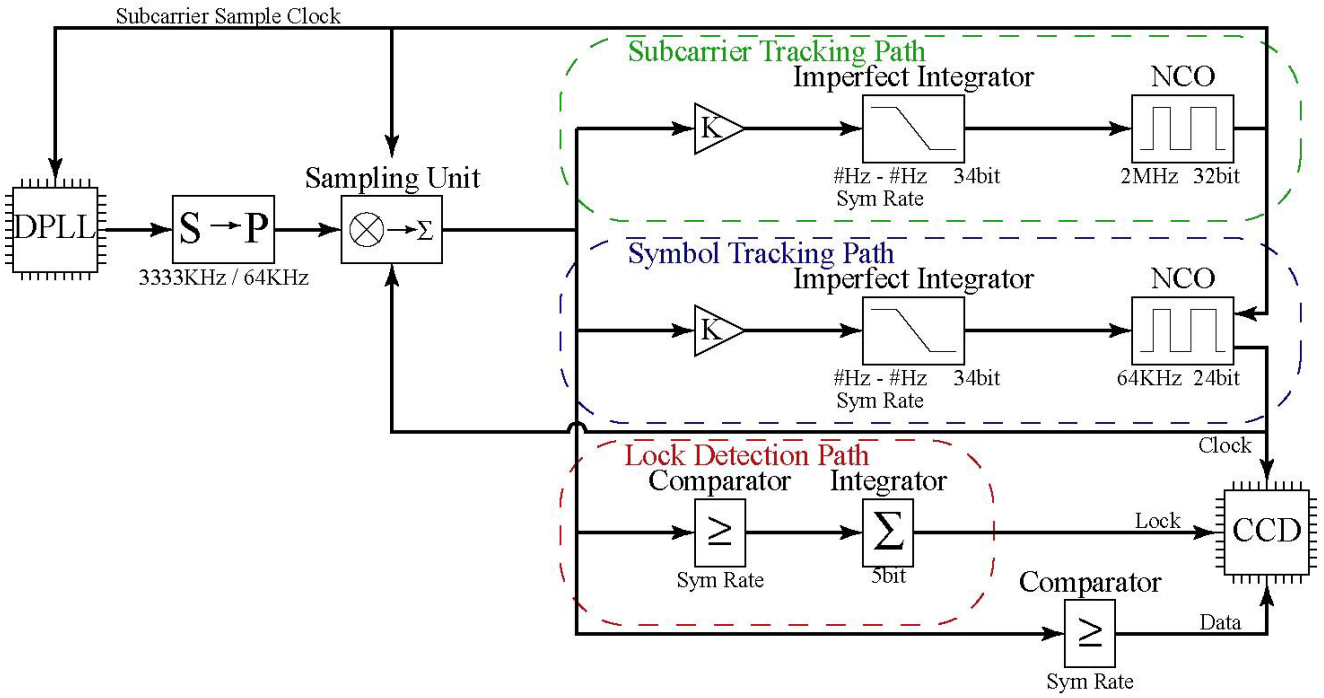

Figure 7 - CDU Block Diagram

channels, and integrated over the symbol period (1/2000, 1/500, 1/125, or 1/7.8125 s). The entire CDU algorithm is executed once over this period. The I channel is used as the phase error input to the Subcarrier Tracking Path. The Sampling Unit also outputs 2 subsets of the peaks integration value, one integration set spanning a short time just before the start of a new symbol and one just after. The Symbol Tracking Path uses these values to perform early/late-gate synchronization to the symbol pattern [3]. Both the Subcarrier and Symbol Tracking Paths use the same Imperfect Integrator circuit as the DPLL Carrier Tracking Path, and work simultaneously to track the uplink signal. The time constants of the Imperfect Integrator change with symbol rate to obtain the lowest command threshold possible at 7.8125 bps and reasonable track rate at higher symbol rates. The Lock Detection Path compares the Q channel values to a threshold at the symbol rate. The single bit output of the threshold test is then sent into a limited integrator, which applies a smoothing function to the lock bit.

5. Performance Highlights

The primary performance achievement of the new digital receiver system is low power consumption. In addition, several major performance improvements were made as a result of the new design approach, such as improved carrier tracking and command threshold, temperature performance, and mass. The new design also fully meets all new requirements needed for proper operation of the REX radioscience and Regenerative Ranging subsystems. **Table 1** illustrates these performance achievements and improvements relative to the CONTOUR X-band Uplink Receiver. A significant power savings over commercially available X-band deep space transponding systems (SDST) has been made, which draw approximately 8.9W secondary power (approximately 11.9W primary power, 75% efficiency assumed) in receive only mode (not including a CCD)[8]. Based on these numbers, a 53% to 68% reduction in secondary power consumption over comparable predecessor systems has been achieved while maintaining similar or better performance and improved capability and flexibility.

Other, more qualitative, improvements were also made due to the new design approach. The use of a DDS and digital loop filter as the carrier tracking frequency source instead of a VCO or dielectric resonator oscillator (DRO) and analog filter removes all temperature effects on the best lock frequency (BLF) accuracy and carrier tracking loop performance. BLF telemetry information to 0.5 Hz at X-band may be downlinked to aid operations. Also, since the AGC system uses a digital power detection circuit, temperature-induced variation in the AGC voltages and gain is eliminated. The net result due to the elimination of these temperature effects is in improved carrier acquisition threshold at temperature extremes. Finally, circuits in the digital subsystem have been digitally optimized to maximize receiver performance; this digital optimization process eliminates uncertainties and repeatability problems in the tuning and assembly process and opens up the potential capability for in-flight optimization of various circuits for other missions.

6. Conclusions and Future Work

This paper gives a somewhat qualitative overview of the new X-band Uplink Receiver design. Several major performance parameters of the operational and functional RF uplink system have been improved upon compared to

Table 1 – Performance Highlights and Improvements of the New Horizons X-band Digital Receiver
(SEL=single event latchup, LET=linear energy transfer threshold)

Parameter	New Horizons	CONTOUR
Mass	550 grams (to be updated)	670 grams
Secondary Power	2.8 W (including CCD) (to be updated)	6 W (including CCD)
Temperature	-35° to +85° C operating range	-35° to +85° C operating range
Noise figure (w/external LNA/filter)	1.5 dB (25 ° C)	< 2.0 dB
BLF settability and stability	< +/-0.1 ppm over full temperature range relative to USO stability	+/-10 ppm over full temperature range, relative to USO stability
Carrier acquisition threshold	-157 dBm at BLF over full temperature range	-155 dBm typical, -150 dBm worst case over full temperature range
Dynamic range	-157 to -50 dBm (operating within spec) -157 to 0 dBm (no damage)	-155 to -70 dBm (operating within spec) -155 to 0 dBm (no damage)
Acquisition sweep rate	>2800 Hz/sec @ ≥ –100 dBm carrier power >1800 Hz/sec @ ≥ –120 dBm >650 Hz/sec @ ≥ –130 dBm	>400 Hz/sec @ ≥ –130 dBm
Pull-in range	>+/- 1.3 KHz @ -120 dBm	>+/- 1.3 KHz @ -120 dBm
Tracking range	+/- 250 kHz centered on BLF	+/- 150 KHz centered on BLF
BER performance (P_e= 10^{-5})	< 3 dB from theory at 2000 bps < 1 dB from theory at 7.8125, 125, 500 bps	Strong signal only at 2000 bps < 3.5 dB from theory at 7.8125 < 1 dB from theory at 125, 500
Ranging channel	DSN sequential tone system and PN	DSN sequential tone system only
Uplink Radioscience Mode	YES (REX)	NO
Standardized frequency reference	YES (30.0 MHz, but not limited to this)	NO, 30.6 MHz
Radiation Immunity Mission Requirement	Total ionizing dose ≥ 15 Krads(Si) SEL immune to LET ≥ 80 MeV-cm^2/mg	Total ionizing dose ≥ 8 Krads(Si) SEL immune to LET ≥ 120 MeV-cm^2/mg

predecessor systems, including low power consumption, improved carrier tracking and command threshold, performance at temperature extremes, and mass. The leveraging of enabling commercial technologies mixed with in-house development of critical components has resulted in a highly efficient system with improved performance over predecessor systems. The use of digital circuitry coupled with a new approach to solving an old problem is clearly the foundation for this new design.

One of the key benefits of adding the digital subsystem to this design is in operational flexibility. Once in place, successive design iterations in future missions may include in-flight reconfiguration of RF channel reassignments, carrier tracking loop optimization for near-Earth, deep space, and interstellar operational modes, and so on. A secondary benefit of more digital systems is in the ability to leverage from increasing gate array densities and processing unit speeds, thus contributing to further mass, size, and power savings. Finally, further reduction in hardware assembly due to lower parts count and solder connections increases the reliability of these systems.

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BIOGRAPHY

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